IN THE CLAIMS

Please amend the claims as follows:

Claims 1-28 (Canceled).

Claim 29 (Previously Presented): A semiconductor memory device comprising:

a semiconductor substrate;

a first element isolating insulation film and a second isolating insulation film, for isolating an element region;

a first gate electrode including a first portion having a side surface in contact with a side surface of the first element isolating insulation film and a second portion having a side surface aligned with the side surface of the first portion of the first gate electrode, the second portion projecting from an upper surface of the first element isolating insulation film;

a second gate electrode including a first portion provided on the first gate electrode with a first insulation film interposed therebetween and a second portion extending on the first element isolating insulation film, the second portion having a thickness different from that of the first portion of the second gate electrode; and

a resistance element provided on the second element isolating insulation film with a second insulation film interposed therebetween, the resistance element being formed of a same material as that of the second gate electrode and not extending on the element region, the second insulation film being formed of a same material as that of the first insulation film.

Claim 30 (Canceled).

Claim 31 (Currently Amended): A semiconductor memory device comprising:

a semiconductor substrate;

a first element isolating insulation film and a second isolating insulation film, for isolating an element region, the second element isolating insulation film having a part having a same height as that of the first element isolating insulation film, and the second element isolating insulation film having an upper surface higher than that of the first element isolating insulation film;

a first gate electrode including a first portion having a side surface in contact with a side surface of the first element isolating insulation film and a second portion having a side surface aligned with the side surface of the first portion of the first gate electrode, the second portion projecting from an upper surface of the first element isolating insulation film;

a second gate electrode including a first portion provided on the first gate electrode with a first insulation film interposed therebetween and a second portion extending on the first element isolating insulation film, the second portion having a thickness different from that of the first portion of the second gate electrode; and

a resistance element provided on the second element isolating insulation film, the resistance element being formed of a same material as that of the second gate electrode and not extending on the element region.

Claims 32-33 (Canceled).

Claim 34 (Previously Presented): The device according to claim 29, wherein the second element isolating insulation film has an upper surface higher than that of the first element isolating insulation film.

Claim 35 (Previously Presented): The device according to claim 29, wherein the second portion of the second gate electrode and the resistance element are isolated from each other on the second element isolating insulating film.

Claim 36 (Previously Presented): The device according to claim 29, wherein the first gate electrode is a floating gate of a non-volatile semiconductor memory, and the second gate electrode is a control gate electrode.

Claim 37 (Previously Presented): The device according to claim 29, wherein the resistance element is part of a peripheral control circuit provided on a periphery of a memory cell array region.

Claim 38 (Canceled).

Claim 39 (Previously Presented): The device according to claim 31, wherein the second portion of the second gate electrode and the resistance element are isolated from each other on the second element isolating insulation film.

Claim 40 (Previously Presented): The device according to claim 31, wherein the first gate electrode is a floating gate of a non-volatile semiconductor memory, and the second gate electrode is a control gate electrode.

Claim 41 (Previously Presented): The device according to claim 31, wherein the resistance element is part of a peripheral control circuit provided on a periphery of a memory cell array region.

Claim 42 (Previously Presented): A semiconductor memory device having a cell section and a peripheral section comprising:

a semiconductor substrate;

a first element isolating insulation film provided in the cell section;

a second element isolating insulation film provided in the peripheral section;

a first gate electrode including a first portion having a side surface in contact with a side surface of the first element isolating insulation film and a second portion having a side surface aligned with the side surface of the first portion of the first gate electrode, the second portion projecting from an upper surface of the first element isolating insulation film;

a second gate electrode including a first portion provided on the first gate electrode with a first insulation film interposed therebetween and a second portion extending on the first element isolating insulation film, the second portion having a thickness different from that of the first portion of the second gate electrode; and

a resistance element provided on the second element isolating insulation film with a second insulation film interposed therebetween, the resistance element being formed of a same material as that of the second gate electrode, the second insulation film being formed of a same material as that of the first insulation film.

Claim 43 (Previously Presented): The device according to claim 42, wherein the second element isolating insulation film has an upper surface higher than that of the first element isolating insulation film.

Claim 44 (Previously Presented): The device according to claim 42, wherein the second portion of the second gate electrode and the resistance element are isolated from each other on the second element isolating insulation film.

Claim 45 (Previously Presented): The device according to claim 42, wherein the first gate electrode is a floating gate of a non-volatile semiconductor memory, and the second gate electrode is a control gate electrode.

Claim 46 (Previously Presented): The device according to claim 42, wherein the resistance element is part of a peripheral control circuit provided on a periphery of a memory cell array region.

Claim 47 (Previously Presented): The device according to claim 42, wherein the second element isolating insulation film has a part having a same height as that of the first element isolating insulation film.